Remarks

Claims 1-14 are pending in this action. Claims 1-14 stand rejected. By this amendment claim1 has been amended. Applicants respectfully request reconsideration of all pending claims herein.

Claim Objections

The Office Action stated that Claims 1 – 14 are objected to because "a memory block located at each of the cross points" is unclear because memory location seems to be irrelevant in the claim, contrary to the memory connection/association to the ports as claimed. Applicants have amended Claim 1 to clarify that a memory block is associated with an input port and an output port and is not dependent on physical location. Claim 1 now reads, "...wherein the packet switch comprises a plurality of memory blocks, each memory block associated with one of said cross points ...".

Therefore, Applicants believe that the objection to claims 1-14 has been overcome.

Claim Rejections - 35 U.S.C. § 112, second paragraph

The Office Action stated that claims 1-14 are rejected under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as his invention. Specifically, for Claim 1, the Office Action stated that it was unclear as to what output and input ports are considered a pair and what is the definition of a cross point. Applicants submit that the definition of "cross point" is defined in paragraph 10 of the specification as "each couple of an input port and an output port defining a cross point within the switch module" and is shown in Figures 1, 3, 5, and 8. In Figure 1, the input and output ports are shown as the input buses 13_1 – 13_4 and corresponding output busses 15_1 – 15_4 coupled

to the packet switch module 14. A pair is therefore any one of the input ports (i.e. input bus 13) coupled to any one of the output ports (i.e. output bus 15). For example, one cross point is input bus 13_1 coupled to output bus 15_4, or input bus 13_2 coupled to output bus 15_3, etc. Thus, for 4 input ports and 4 output ports there is a total of 16 cross points. In Figure 3 the cross point is shown as the intersection of elements 50 and 60, which are coupled to data bus in 13 and data bus out 15 respectively (see paragraph 27). Memory Block 200 is associated with the cross point shown in Figure 3. Figure 5 shows a block diagram of Memory Block 200 with the intersection of elements 50 and 60 showing the cross point. Figure 8 shows multiple cross points for input ports 13_1 – 13_m and output ports 15_1 – 15_m and represents an mxm number of cross points with associated memory blocks 200 for each cross point.

The Office Action stated that the limitation in claim 1 of "... selecting at each clock time ..." is unclear because it is not understood when the selection should occur, as there are no time units associated with "each clock time". Applicants have amended Claim 1 to replace "each clock time" with "each clock cycle", which is a well-known term in the networking and computer industries.

Based on the foregoing arguments and amendments, Applicants believe that the rejection to Claims 1 – 14 under 35 U.S.C. §112, second paragraph, has been overcome.

Claim Rejections - 35 U.S.C. § 103(a)

The Office Action stated that claims 1, 2 and 10 are rejected under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 6,205,145 issued to Yamazaki.

Applicants respectfully submit that the present invention is patentable over U.S. Patent No. 6,205,145 issued to Yamazaki because Yamazaki does not teach or suggest the limitation of Applicants' claim 1, as amended, of " ... the packet switch comprises a plurality of memory blocks,

each memory block associated with one of said cross points ... ". Support for Applicants' claim 1, as amended, can be found, for example, in paragraph 0025 and Figure 3.

The combination of input and output buffer means shown as 20-23 and 30-33 respectively on Fig. 5 of the Yamazaki reference are not cross points because there is no provision for each input/output buffer combinations to coordinate one-to-one with every termination node input/output node combination. Yamazaki does not teach a memory block for each of the cross points because cell producing means 40-43 does not include a first memory controller which determines from the packet header whether the packet is to be forwarded to the output port associated with the cross point. Rather, the frame division control section 143 of Figure 8 (referred to in the Office Action) serves to divide an incoming packet into fixed length cells, interchange the cells and, reconstruct the original frame from the interchanged cells (See Yamazaki Abstract, Summary, Claims 1, 6, 10, 16, 26, and 29, Figure 8, and 10:57-11:4). The output buffer requirement control section 144 of Figure 8 sends command signals the frame division control 143 according to inputs from the congestion control bus 180 (See Yamazaki 10:14-26, and Figures 6 and 8). Neither the output buffer requirement control section 144 nor the frame division control section 143 determine from the packet header whether the packet is to be forwarded to the output port associated with the cross point as taught by the Applicants' instant invention.

Applicants respectfully submit that Yamazaki does not teach or suggest the limitation of Applicants' claim 1, as amended, of "...a plurality of schedulers, each scheduler associated with one of said output ports ...". Support for Applicants' claim 1, as amended, can be found, for example, in paragraphs 0008, 0026, 0051, 0052 and Figures 3 and 8.

Referring to Figure 5 of Yamazaki, Yamazaki teaches a single congestion control means 70 associated with a plurality of frame construction means 50-53 and, indirectly, a plurality of output data buffer means 30-33. Yamazaki's congestion control means 70 is unique and centralized in the fibre channel fabric so the congestion control means 70 must know the complete switching topology of the system in order to control packet flow. Yamazaki is silent on teaching or suggesting a plurality of congestion control means, each congestion control means associated with one of the output data buffer means.

Therefore, Applicants believe that the rejection of Claims 1, 2 and 10 under 35 U.S.C. §103(a) has been overcome.

Conclusion

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
For: Alain Benayoun, et al.

By: _____

Anthony J. Canale
Registration No. 51,526
Telephone No.: (802) 769-8782
Fax No.: (802) 769-8938
EMAIL: acanale@us.ibm.com

International Business Machines Corporation
Intellectual Property Law - Mail 972E
1000 River Road
Essex Junction, VT 05452